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Modified 9-98

PTO/SB/21 (12-97)

Approved for use through 9/30/00. OMB 0651-0031

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**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

BOX:

Express Mail
Receipt No.

Application / Conf. No.

10/086,129 / 2232

Filing Date

February 28, 2002

First Named Inventor

David P. Schultz

Examiner Name

Unknown

Group Art Unit

2133

Issue Fee Batch No.

Attorney Docket Number

X-1069 US

RECEIVED

OCT 21 2002

Technology Center 2100

ENCLOSURES (check all that apply)☒ Fee Transmittal Form☒ Amendment / Response☒ Preliminary Amendment☐ After Final☐ Affidavit(s)/declaration(s)☐ Extension of Time Request☐ Change Status to LARGE ENTITY☐ Express Abandonment Request☐ Information Disclosure Statement☐ Substitute PTO-1449(s)
IDS by Applicant (PTO/SB/08A)☐ Certified Copy of Priority
Document(s)☐ Response to Missing Parts/
Incomplete Application☐ Response to Missing
Parts under 37 CFR
1.52 or 1.53☐ Assignment Papers
(with Recordation Cover Sheet)☐ Declaration / Oath☐ Drawing(s)☐ Licensing-related Papers☐ Petition -☐ To Convert a
Provisional Application☐ Power of Attorney, Revocation
Change of Correspondence
Address☐ Terminal Disclaimer☐ Request for Refund☐ After Allowance Communication
to☐ Appeal Communication to Board
of Appeals and Interferences☐ Appeal Communication to Group
(Appeal Notice, Brief, Reply Brief)☐ Status Letter☒ Return Receipt Postcard☐ Additional Enclosure(s)
(please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENTFirm or
Customer Number

Attn:

H. C. Chan

24309

(Customer Number)

Reg. Number 35,477

Signature

Date

October 10, 2002

Charge any additional fees required/credit any overpayment
to our Deposit Account Number: **24-0040****CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D. C. 20231 on this date: October 10, 2002

Typed or Printed Name

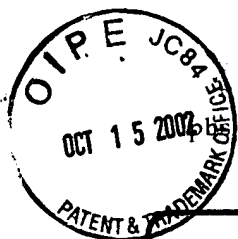
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Date

October 10, 2002

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT (\$ 210.00

Complete if Known

Application / Conf. No.	10/086,129 / 2232
Filing Date	February 28, 2002
First Named Inventor	David P. Schultz
Examiner Name	Unknown
Group / Art Unit	2133
Attorney Docket No.	X-1069 US

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees, any additional fees required, and credit any over payments to:

Deposit
Account
Number

24-0040

Deposit
Account
Name

XILINX, INC.

- ☐ Charge the any additional Fee Required
Under 37 CFR §§ 1.16 and 1.17

2. ☐ Payment Enclosed:

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity

Fee Code	Fee (\$)	Fee Description	Fee
101	740	Utility filing fee	
106	330	Design filing fee	
107	540	Plant filing fee	
108	710	Reissue filing fee	
114	150	Provisional filing fee	

SUBTOTAL (1)

(\$)

2. EXTRA CLAIM FEES

Total Claims	Extra	below	Fee Paid
-20**	27	7	18
Indep. Claims	06	1	84
Multiple Dependent Claims			

**or number previously paid, if greater; For Reissues, see below

Large Entity

Fee Code	Fee (\$)	Fee Description
103	18	Claims in excess of 20
102	84	Independent claims in excess of 3
104	270	Multiple dependent claim, if not paid
109	84	**Reissue independent claims over original patent
110	18	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)

(\$)

210.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity

Fee Code

Fee (\$)

Fee Description

105	130	Surcharge - late filing fee
127	50	Surcharge - late provisional filing fee or cover sheet.
147	2,520	For filing a request for expedite reexamination
112	920*	Requesting publication of SIR prior to Examiner action
113	1,840*	Requesting publication of SIR after Examiner action
115	110	Extension for reply within first month
116	400	Extension for reply within second month
117	920	Extension for reply within third month
118	1,440	Extension for reply within fourth month
128	1,960	Extension for reply within fifth month
119	320	Notice of Appeal
120	320	Filing a brief in support of an appeal
121	270	Request for oral hearing
138	1,510	Petition to institute a public use proceeding
140	110	Petition to revive - unavoidable
141	1,240	Petition to revive - unintentional
142	1,280	Utility issue fee (or reissue)
122	130	Petitions to the Commissioner
123	50	Petitions related to provisional applications
126	180	Submission of Information Disclosure Stmt
581	40	Recording each patent assignment per property (times number of properties)
146	740	Filing a submission after final rejection (37 CFR 1.129(a))
149	740	For each additional invention to be examined (37 CFR 1.129(b))
179	740	Request for Continued Examination (RCE)

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

(\$)

SUBMITTED BY

Name (Print/Type)

H. C. Chan

Registration No.
(Attorney/Agent)

35,477

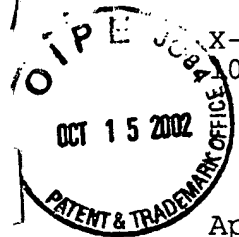
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X-1069 US
10/086,129

PATENT
Conf. No. 2232

#4/A
10-25-02
M.L.

IN THE UNITED STATES PATENT OFFICE

Applicant: David P. Schultz
Assignee: Xilinx, Inc.
Title: Method and System for Flexibly Nesting JTAG TAP
Controllers for FPGA-Based System-On-Chip (SoC)
Serial No.: 10/086,129 File Date: 2/28/2002
Examiner: Unknown Art Unit: 2133
Docket No.: X-1069 US Conf. No.: 2232

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

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PRELIMINARY AMENDMENT

Dear Sir:

Before taking action in the above-referenced case, please
make the following amendments to the claims.

IN THE CLAIMS

Please replace Claim 14 with the following:

14. (Amended) A system for flexibly accessing nested JTAG TAP
controllers for IP cores in a FPGA-based SoC, the system
comprising:

A1 a selector for choosing at least one IP core JTAG TAP
controller from a plurality of JTAG TAP controllers nested in
the FPGA-based SoC; and

a multiplexer for programmably connecting said at least one
IP core JTAG TAP controller to a host JTAG TAP controller.

Please add Claims 21-27 as follows:

21. (New) A system for performing boundary scan functions on a
plurality of IP cores, the system comprising:

A2
Cm.T an FPGA-based system-on-chip (SoC) comprising a plurality
of IP cores each including a first JTAG TAP controller; and

10/17/2002 SSITHIB1 00000084 240040 10086129

01 FC:1201 84.00 CH
02 FC:1202 126.00 CH